SYLLABI OF COURSES FOR DIPLOMA PROGRAMME IN MEDICAL ELECTRONICS, LEVEL IV & V

		4134	- DIGI	TAL	ELECTR	ONIC	S-1				
				-	Examination Schedule (Marks)						
Teaching Schedule Per Week			Progressive Assessment			Theory			Practical Ex.		
Lectures	Practical	Credits						50		200	
3	2	5	25	25	3 Hrs					Gr Tota	
Pre-requisite		Source	Semester		Theory	Test	Total	TW	SD SD	175	
		EXN	Sem	ester	75	25	100	as	120	175	

Rationale: This course introduces the basics to Digital world. So study of Karnaugh mapping techniques, flip-flops, registers and counters becomes very essential.

ps, registers and	Hrs	Mks
COURSE CONTENTS	6	10
 NUMBER SYSTEM AND CODES Concept of digital and analogue signals, binary, decimal, octal and hexadecimal number system, conversion from one system to another, BCD codes, ASCI code, Gary code, Binary Addition, Subtraction, 1's compliment, 2's compliment methods, Duality, Positive and Negative logic systems. 	9	20
2. BOOLEAN ALGEBRA AND LOGIC GATES Principles of Boolean algebra and De Morgan's theorems, symbol, basic sancepts,		ī.
Implementation of simple logic expression	9	20
 FLIP- FLOP Principle of operation schematic and truth tables of basic flip flop RS FF, DFF, JK FF, JK Master FF, T FF. 	12	25
4. REGISTERS AND COUNTERS Concept of sequential and combination digital systems. Principles of operation, schematic of shift registers various modes of operation. Principles of operation, schematic of counters such as synchronous and asynchronous counters, ripple, up, down, and up down, BCD, decade, mod, ring counter. Simple application of up down, action with registers.	12	. 25
 counters and shift registers. 5. DIGITAL LOGIC FAMILIES Characteristics of digital ICs- flexibility, speed, power, and noise considerations, famin, and fan-out. RTL, DCTL, DTL, HTL characteristics. TTL, TTL series and characteristics. ECL, MOS, CMOS, logic gates. Tristate logic CTL, I2I and ECL comparison between various logic families. 		8 10
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Students are required to perform any eight experiments from the following.
Verification of logic gates.
Study of Universal gates.

Study of Universal gates.
 Verification of De Morgan's Theorem.
 Verification of Boolean expression.
 Construction and testing of RS FF, Clocked RS FF using gates.
 Construction and testing of JK FF, JK MS FF, DFF, TFF.
 Conversion of Gary Code to Binary and Vice Versa using gates.

HUMAN RESOURCE & CURRICULUM DEVELOPMENT CELL, DIRECTORATE OF TECHNICAL EDN, GOA.VL-XIV, 11-2000

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SYLLABI OF COURSES FOR DIPLOMA PROGRAMME IN MEDICAL ELECTRONICS, LEVEL IV & V

- Application of XOR gate as Parity Checker.
 Study of following Counter using ICs: a) UP, b) down, c) Up-down, d) Mod-K, e) Frequency divid
- 10. Study of following synchronous counters: a) Binary, b) Decade. 11. Study of following shift registers using ICs: a) SISO, b) SIPO, c) PISO, d) PIPO.

- REFERENCE BOOKS: 1. Micro-electronics by Mihman and Grabel. 2. Digital Computer Fundamentals by Bartee. 3. Pulse and Digital Electronics by G. K. Mithal and A.K. Vanwasi. 4. Digital Computer Electronics by Malvino and Leach

