SYLLABI OF COURSES FOR DIPLOMA PROGRAMME IN INSTRUMENTATION & CONTROL ENGG, LEVEL IV & V

6

		4138	- DIGI	<b>FAL</b>	ELEC	T	RONI	CS- II			
Teaching Schedule Per Week			Progressive		e	Examination Schedule (Marks)					
Lectures	Practical	Credits	Assessmen		ıt	Theory		1	Practical Ex. 50		Total 200
3	2	5	25	25 25		Hr	s 100				
Pre-re	quisite	Source			Theor	v	Test	Total	TW	PR	Gr Total
4134		EXN	Semester		75	2	25	100	25	_	125

Rationale: This subject deals with the design of digital circuits using gales and basic Bootean laws which were dealt in digital electronics- I. These digital circuits are basic building blocks of a digital computer i.e. adders, subtractors, decoders, encoders, ADC, DAC and semi-conductor memories which will enable the student to get in depth knowledge of computer hardware.

COURSE CONTENTS	Hrs	6 Mks				
1. COMBINATIONAL CIRCUITS Study the operation of Half adder, full adder, series and parallel adders, half subtractor, full subtractor, adder subtractor, BCD adder, Binary multiplication and division.						
<ul> <li>DECODERS AND ENCODERS</li> <li>Principles of operation of multiplexer, 16 to 1 multiplexer, Nibble multiplexer, Demultiplexer – 1 to 16, Decoder, Decoder Driver, Encoder – Decimal to BCD, Priority, Encoder. IC's 74147, 7448, 7446, 7445, 74154,74157, 74153,74151, 74150, 7442, 74141.</li> </ul>						
3. A TO D AND D TO A CONVERTERS Study of operation of D to A converter using weighed resistor m use of operational amplifier staircase generator, Resolution A and settling time.Principle of A to D conversion using simult counter or staircase Ramp method, continuous conversion, su Linear Ramp method, Dual slope method, Resolution, Accura ADC's.	10 ethod, Ladder network, accuracy, Monotonicity aneous conversion, accessive approximation, acy, conversion time of	20				
4. CLOCKS AND TIMERS Study of clock waveforms, TTL clock circuit, 555 timer-Astable, and monostable, contact Bounce and Debounce circuits						
5. SEMI-CONDUCTOR MEMORIES Study of memory addressing concepts of ROMS, PROMS and EPROMS, RAMS and DRAMS in detail.						
6. PROGRAMMEABLE LOGIC DEVICES Introduction, ROM as PLD, PLA, Input Buffer, AND matrix, OR matrix, Invert matrix, Output Buffer, Programming the PLA, expanding PLA capacity, Appreciation of PLA's, Programmable Array logic, General logic device, PLD, FPGA.						
Total	48	100				
Study of Half Adder and Full Adder using Gates.       Study of Mono         Study of BCD Adder.       Study of Multip         Study of Encoder and Decoder       Study of Multip         Study of Half Subtractor and Full subtractor using       D to A convert         Gates.       Ladder multip         Study of ALU       TEXT BOOK	stable Multivibrator using IC 555 lexer and Demultiplexer generator er using weighted resistor metho ethod.	d and				
Digital Principles & Applications by Malvino & Leach REFERENCE BOOKS:						
1. Modern Digital Electronics by R. P. Jain, 2. Digital Computer Fund	amentals by Bartee.					
		1075/070 20				

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