			4139- (CIRC	UIT DES	(GN					
				Examination Schedule (Marks)							
Teachin	g Schedule P	er Week		Progressive Assessment		Theory			Ex.	Total	
Lectures	Practical	Credit			3 Hrs	10	0			150	
3	2	_5	25	25			Tota	TW	PR	Gr Total	
Pre-requisite		Source	Semester		Theory	Test	TOTA	1 1 1	1		
		EXN ·								Land and	
_ 		1 14- 0	roote CSD	ahilitie	s to analyse	circuits	encou	nted in B	181C E	ectronics and	

	Lectures	Practical	Credit	Asses	36	3 Hrs	10	0			15	0	i	
	3	2	5	25	25	Theory	Test	Total	TW	PR	Gr T	otal		
	Pre-re	quisite	Source	Sem	ester	Theory	1030	10,000						
			EXN ·					L				e and	}	
		This course is	intended to	create cap	abilities	to analyse	circuits	encount	ed in Ba	tonics	Course	es and	_	
	Rationale:	This course is is also helps	in acquiring	experience	e in the	design of the	ne basic	circuits	III Elect	LOHICS	004		1	
	Devices, 11	119 #130 Herbe					100						l	
- ₹ 			COL	RSE CC	NTEN	TS						Mks		
_											10	20		
. 1	. INTROD	UCTION 1	O COMP	DUENT	SELEC	, IIUIV	337 0F F	itings c	hoosin	Or .				
1	Resistors: R	esistors type	es, variable	resistors,	colour	counts, b	JWCI I	unigo, c	noosin	5				
	the resist Inductors: S	ors for a cir	cuit, resisto	r Iaulis. ductore	a and	calculation	n of tur	ns and	core are	ea				
]	inductors: S	elf-inductar en inductan	ice, mutuai .a. Inductivi	e reactan	ce O o	f a core, at	plicati	ons wit	h					
	en 14	Taminal age	acitors colo	ur coding	g, charg	ing and di	scharg	ing of a	capaci	tor.				
	O	tatomos	l'ime cons	เรลหร สทก	ncauoi	IS WILLI CAG	ritthico.	, capac.						
		Climala mb	aga ofen III	cten day	m irans	HOLLICI. L	A Dro OT	COLCOC	010 1000	, ,				
	calculati	ons of prim	ary and seco	ondary tu	rns and	core area	tor 50	Hz-pow	er supp	ny.				
	Typical	applications	with exam	ples.							14	30		
	a novemb	CTIDDI V									1 -7	30		
	2. POWER Designing I	-1 <i>C</i>	ctifier, Full	wave rec	tifier fo	or specifie	d volta	ge and p	ower.	Use				
	1-4-	<i>C</i>	ad output W	alijes SD	เดง ดะ เ	C /23 108	uiawi,	CC31E111						
	~ .	1-+ fa	- airina a/n	VALIAGES	and bu	WCI. COIIC	Chr mr	41301000						`
		1 .1 (alanlations	and desi-	on cons	anerauous	· DALL	TILLY IN A C	5	10				
		D -:4	CITUI and L	พักษาที่	neo rec		Ullast	DILLITETA	,,,	.5				
	SCR for	a given vo	ltage and fir	ring angle	es, Desi	ight of com	Honcu	10,000	Juppi)					
	using T	iac for ligh	t dimmer ar	ia motor	specu v	JOHN OIL					12	25		
	3. AMPLI	FIERS				. 11.0	O4-1-1	i.e. foot	or Dec	ion				
			uits for a sir	igle stage	typica	i amplifie	r, Stati	ultietaa	e RC	ııgıı				
	of discr	ete and inte	grated power	er ampuu	iei. Des	sign or typ	icas in	unusung						
	amplifi	er for specif	fied voltage	and curr	ens.						12	25		
	4. OSCIL	LATORS				· σ · 1 C ·		and walt	200					
	Designing	of RC phas	e shift Osci	llators fo	r a spec	torn and I	nency a	for a sp	age. ecifi e d					
	Design	of RC phasing a stable acy and volt	multi-vibra	tor using	Tansis	oscillator	using !	UJT and	PUT	or a				
	frequer	cy and volted saw-toot	age. Design	ing a rea	axamon nev De	signing, U	ntegrati	ing and						
	specific	ed saw-toot	n voltage at	C compo	nents.	.0.6								
	differe	ntiating circ	cuit using K		_						48	100		
				1	otal								_	
	DD 4 OTIO	ALS: (An	v 6)							(No.	Of tur	ns)		
	1 Design	ing a zener	regulator to	or specifi	ed I, V,	P/ratings.					(2)			
	1. Design	ing of 723	regulator fo	r specifie	d ratin	gs.					(2) (2)			
		· - C i	ala statue ar	nniiner c	ii Cuit i	Or obcourse	d ratin	gs.			(4)			
	Λ Design	ing of a mi	inistage RC	, ampirit	r dryon						(3)			
	5 Perfor	mance / rat	ings	•	· . `			v and v	oltage.	*	(3)			
	6. Design	mance / rat	phase shift	oscillator	ior a s	becitter any	IC 55	5 for a s	pecifie	d free	uency	and		
	7. Design	ning of Asta	able Muluvi	ibiator us	ing nu						(2)			
	voltag	e.		:11atos	foras	necified sa	wtootl	ı voltag	e and fi	reque	ncy(2)	,		
		ning of U/I	relaxation	OSCIIIAIOI	rircuite	for specif	ied per	formano	ce					
	Desig	0 _									(2)	١		
	Design	ning Integr	ator / Differ	entiator	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,						(3)	,		
	9. Desig	ning Integra neters.	ator / Diller	entiator		,					(3)	,		
	9. Desig 10. Paran REFERE	ning Integr	oks:	(alvino.							(3	,		