		4222 - 0	COMPU	TER	ORGAN	ISAT	ION - 1	Π			
Teaching Schedule Per Week			Progressive		2	Examination Schedule (Marks)					
Lectures	Practical	Credit	Assessment		t	Theory 3Hrs 100		Practical Ex.		Total	
4	-	. 4			3Hr					125	
Рте-те	quisite	Source			Theory	Test	Tota!	TW	PR	Gr Tota	
4220		COM	Semester		75	25	100		-	100	

Rationale: This course is a continuation of the earlier course in Computer Organisation & deals with Memory & I/O Organisation. Besides Basic Organisation, Interconnection of the above module to the CPU & transfer of data is also dealt with elaborately. A brief study of Pipeline, Vector & Multiprocessing is also introduced.

COURSE CONTENTS		Mks	
1. MEMORY ORGANISATION	8	10	
Main Memory, Ram & Rom chips, Memory Address Map, Memory Connection to the CPU, Auxiliary Memory, Floppy Disks, Hard Disks, Magnetic Tapes, CD ROMS.			
2. RAID TECHNIQUES	8	10	
Associative Memory: Hardware Organisation, Match Logic, Read Operation, Write Operation.	x v		
3. CACHE MEMORY	12	20	
Associative Mapping, Direct Mapping, Set Associative Mapping, Writing into Cache.			
4. VIRTUAL MEMORY	12	20	
Space and Memory Space, Memory Allocation and Mapping. Base & Segment Registers, Paging, Page Replacement, Memory Segmentation.			

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SYLLABI OF COURSES FOR DIPLOMA PROGRAMME IN COMPUTER ENGINEERING, LEVEL IV	/& V	18
5. INPUT - OUTPUT ORGANISATION Input Output Interface: I/O bus and Interface Modules, I/O v/s Memory Bus, I/O Mapped I/O & Memory Mapped I/O.	12	20
Input Output Processor (IOP) : CPU - IOP Communication, Intel 8089 IOP. 6. PIPELINE & VECTOR PROCESSING Pipelining: General Considerations, Arithmetic pipeline, Instruction Pipeline.	12	20
Vector Processing: Vector operations, Matrix Multiplication, Memory Interleaving.		ŧ
Total	64	100

REFERENCE BOOKS: 1. Computer System Architecture by Morris Mano 2. Computer Organisation and System Architecture by Stalling 3. Microprocessor System Design Concept by Nikitas A. Alexandridis 4. Digital Computer Design by V. Rajaraman

